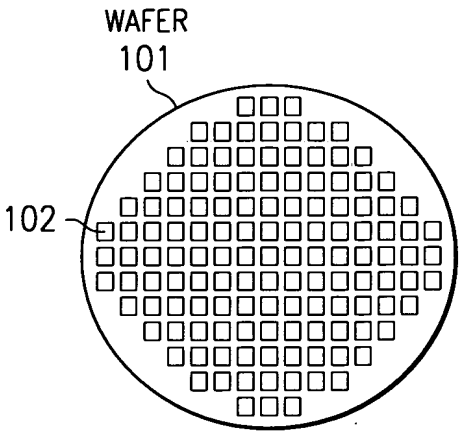


FIG. 1A
(PRIOR ART)

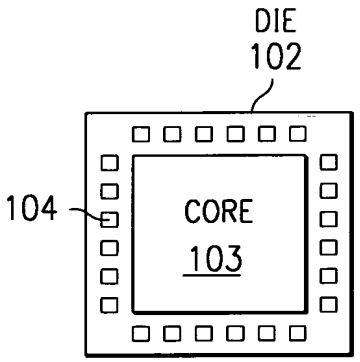


FIG. 1B
(PRIOR ART)

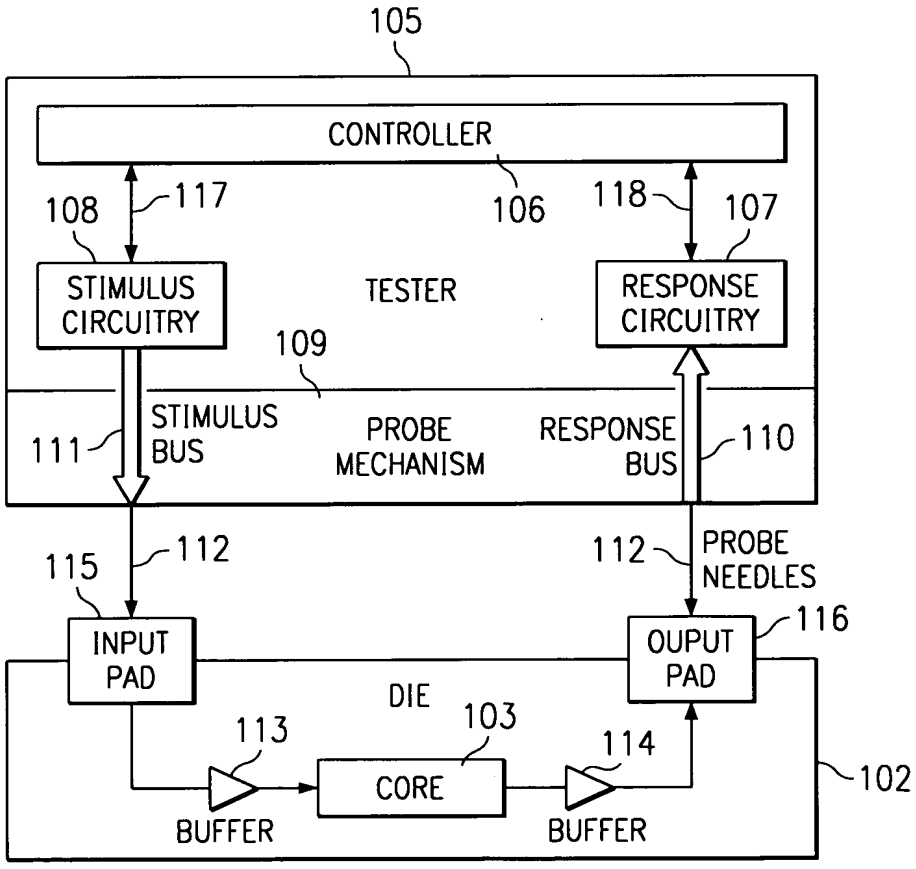


FIG. 1C
(PRIOR ART)

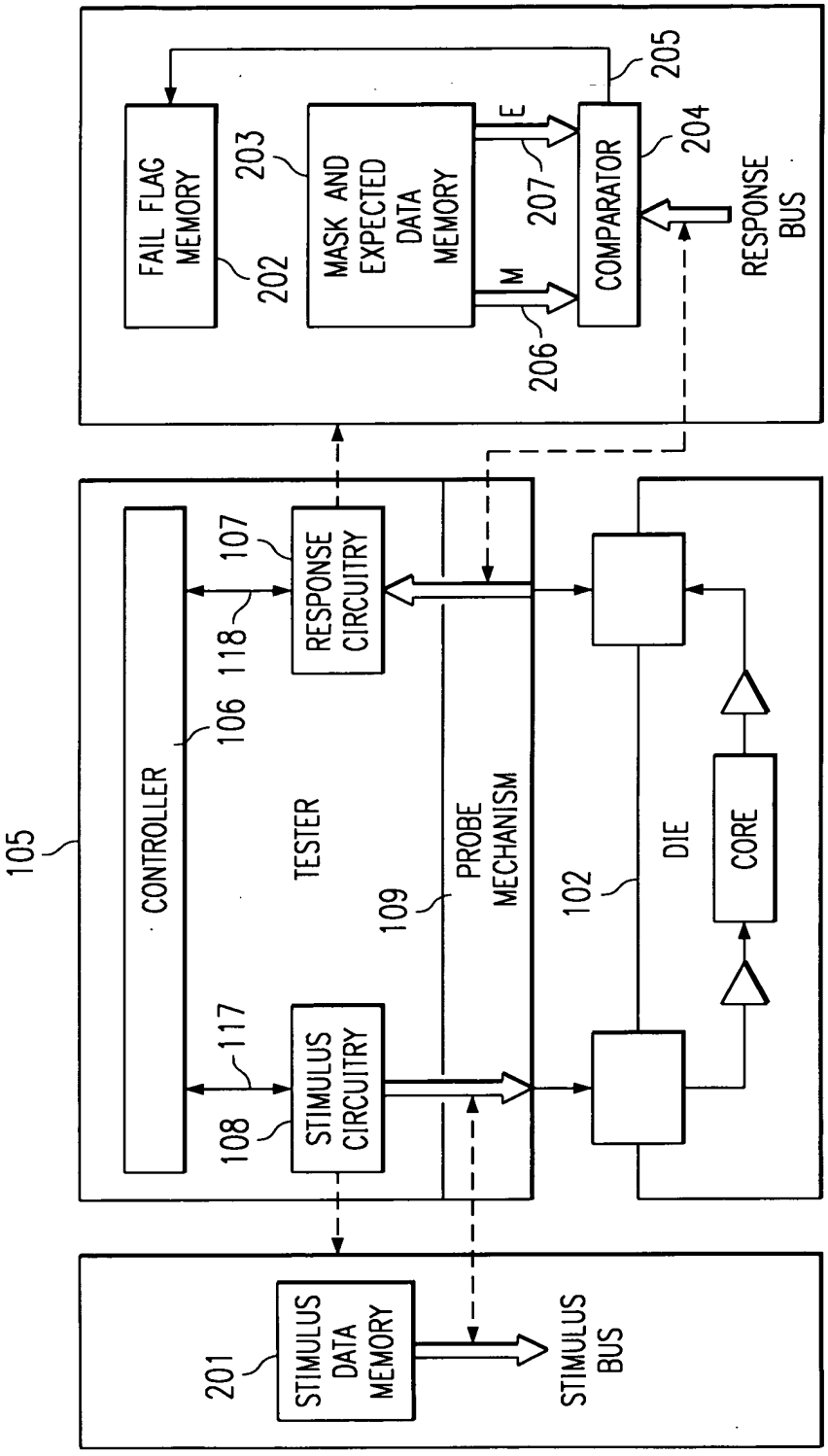


FIG. 2 (PRIOR ART)

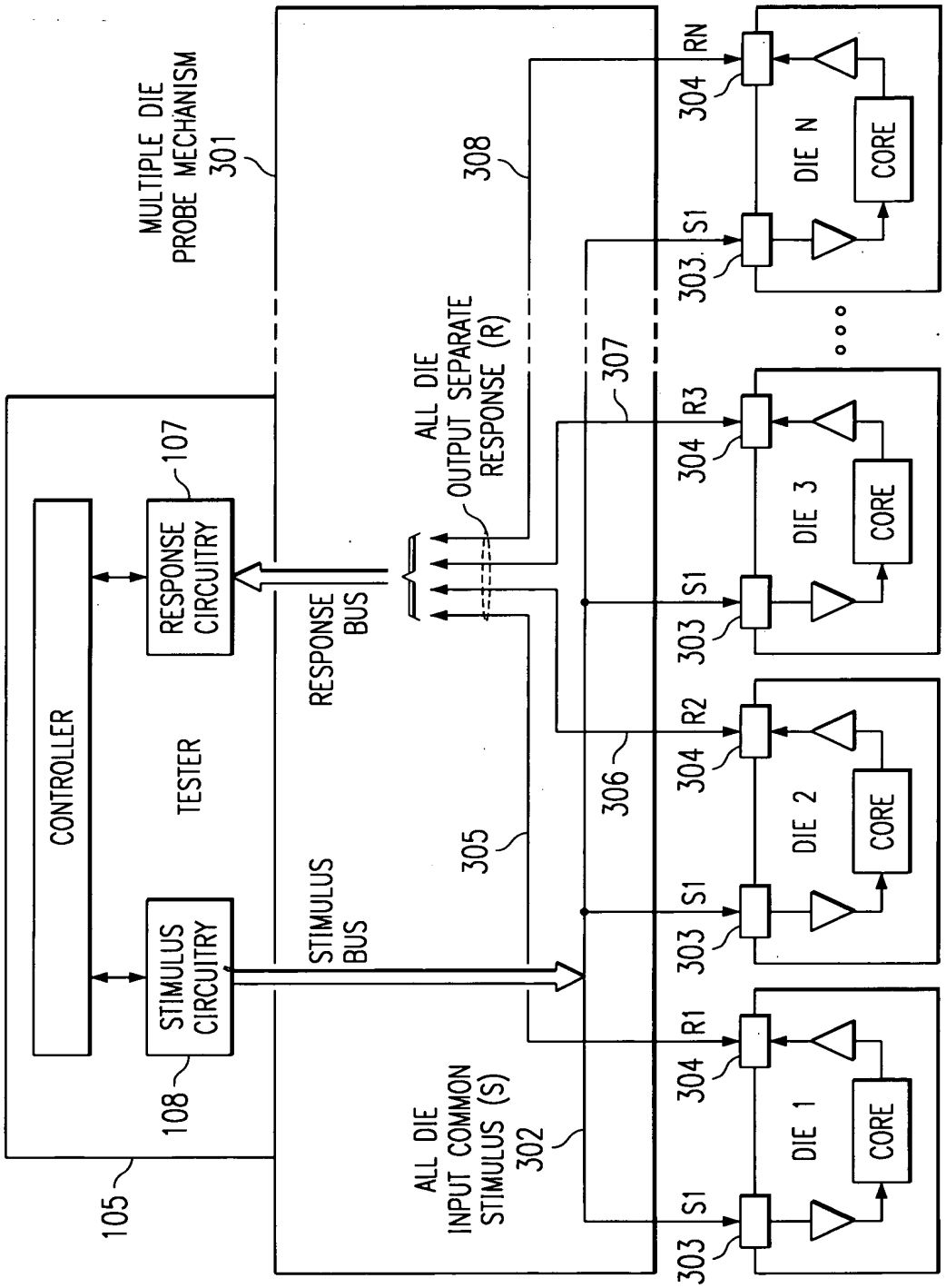


FIG. 3 (PRIOR ART)

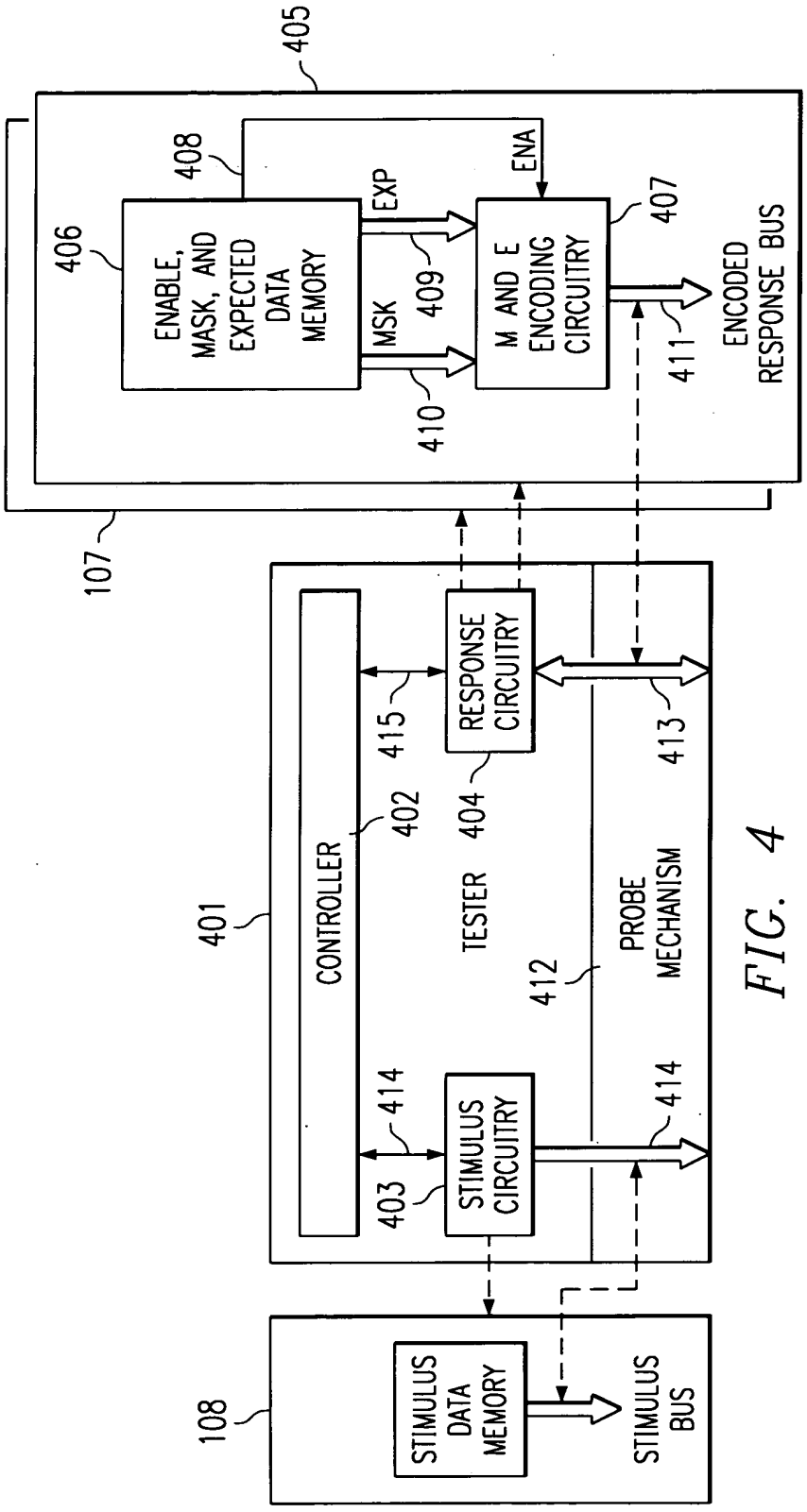


FIG. 4

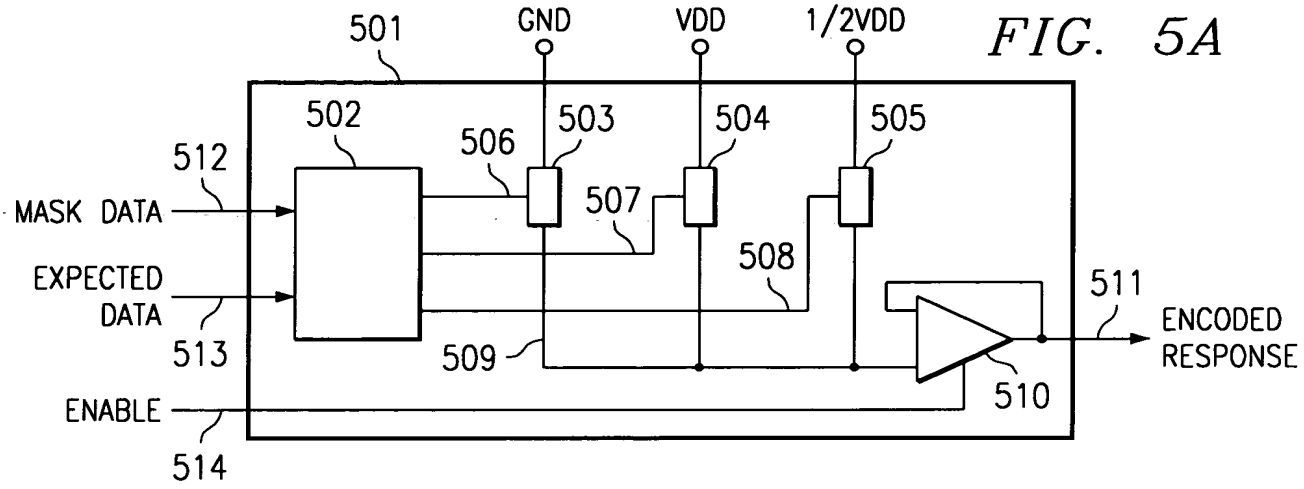


FIG. 5A

FIG. 5B

ENA	MSK	EXP	ENR	OUTPUT MODE
0	0	0	Z	DISABLED
1	0	0	GND	LOW
1	0	1	VDD	HIGH
1	1	X	1/2VDD	MASK

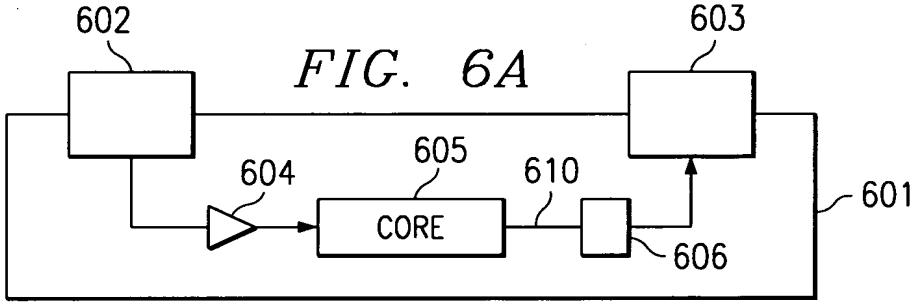


FIG. 6A

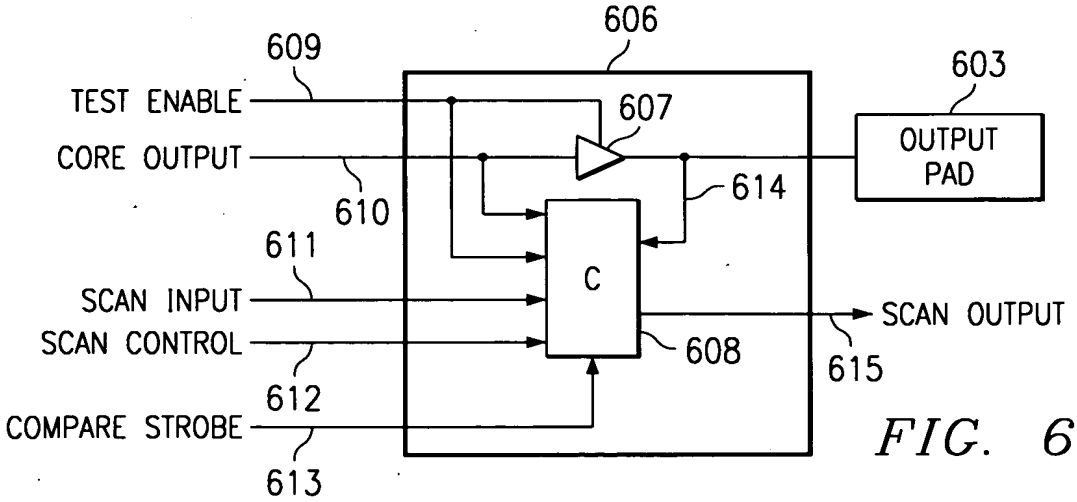


FIG. 6B

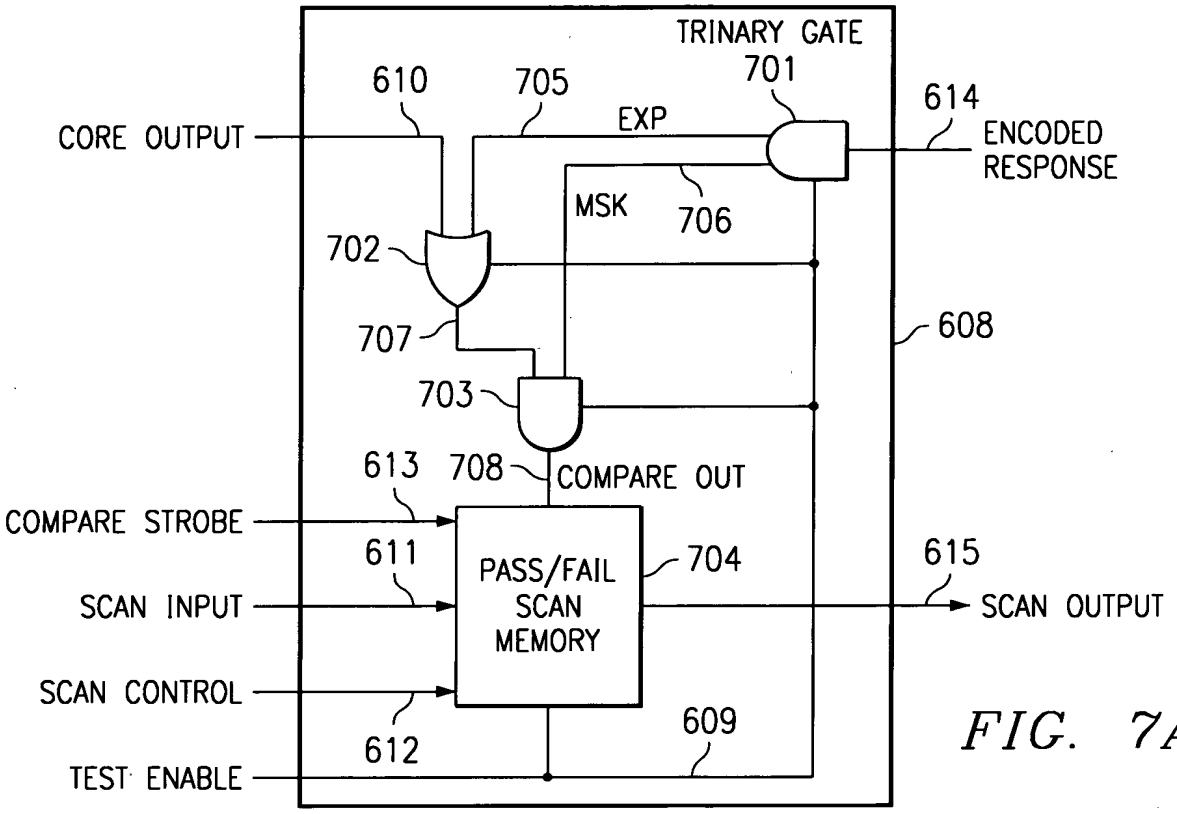


FIG. 7A

TEN	ENR	MSK	EXP	FUNCTION PERFORMED
0	X	X	X	TEST DISABLED
1	GND	1	0	COMPARE LOW
1	VDD	1	1	COMPARE HIGH
1	1/2VDD	0	X	MASK COMPARE

FIG. 7B

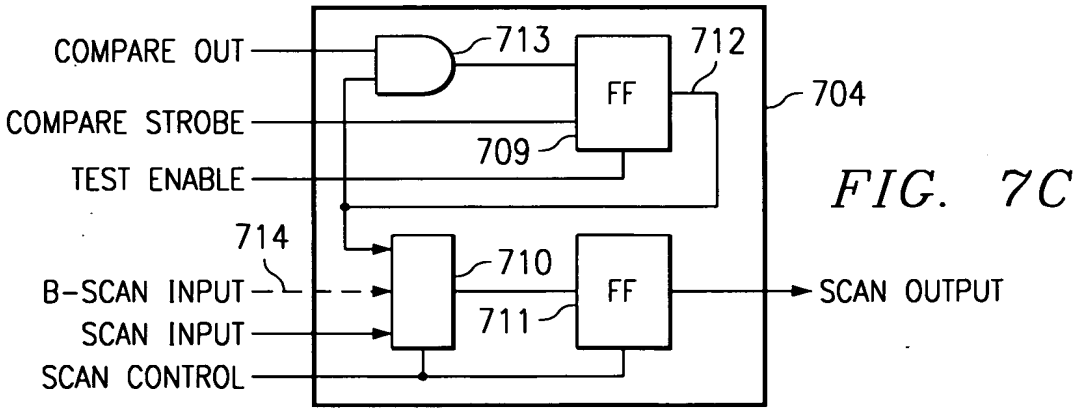


FIG. 7C

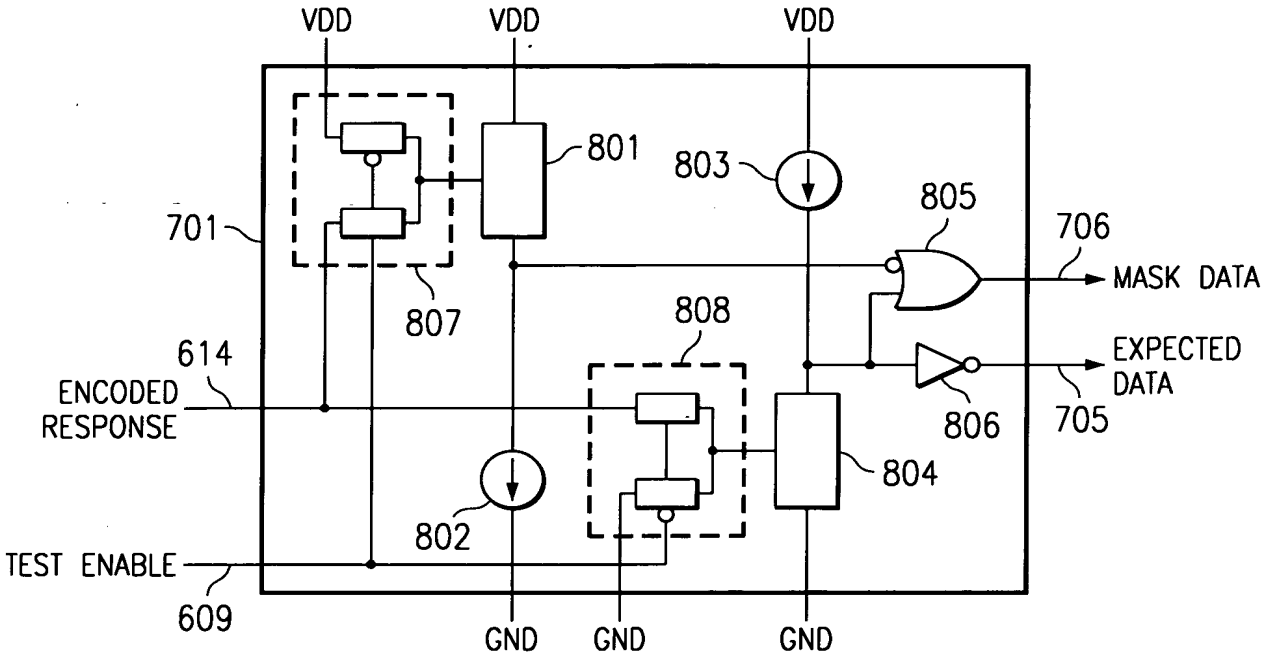


FIG. 8A

TEN	ENR	MSK	EXP	FUNCTION PERFORMED
0	X	1	0	GATE DISABLED
1	GND	1	0	OUTPUT A LOW
1	VDD	1	1	OUTPUT A HIGH
1	1/2VDD	0	X	OUTPUT A MASK

FIG. 8B

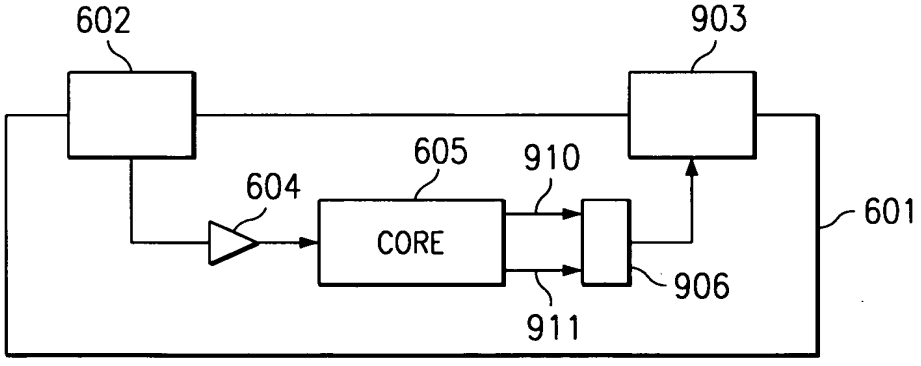


FIG. 9A

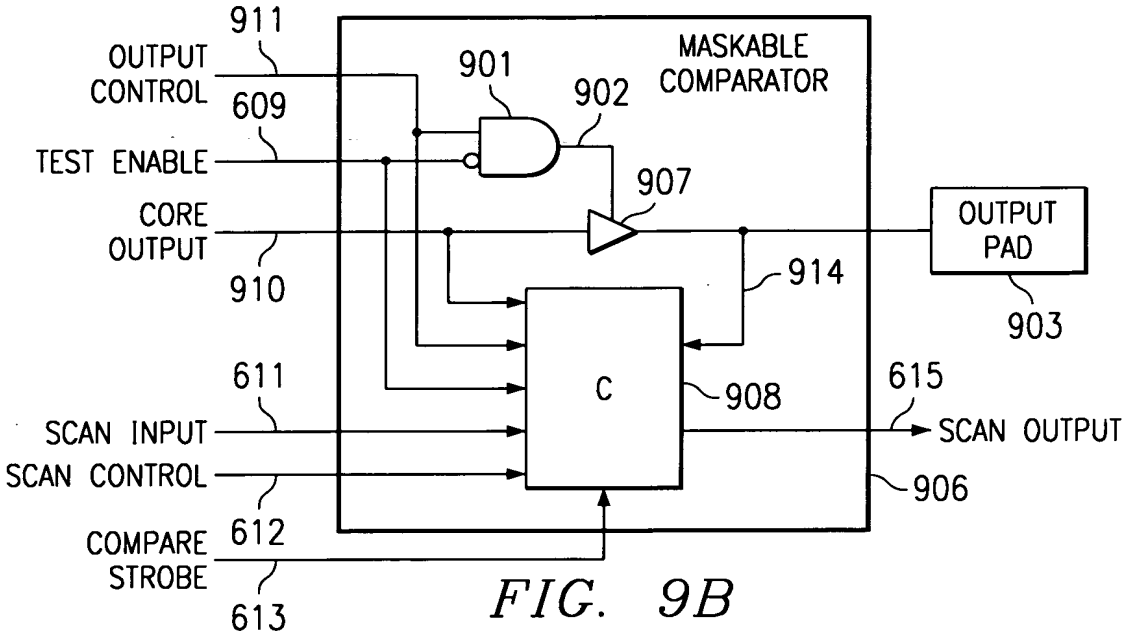


FIG. 9B

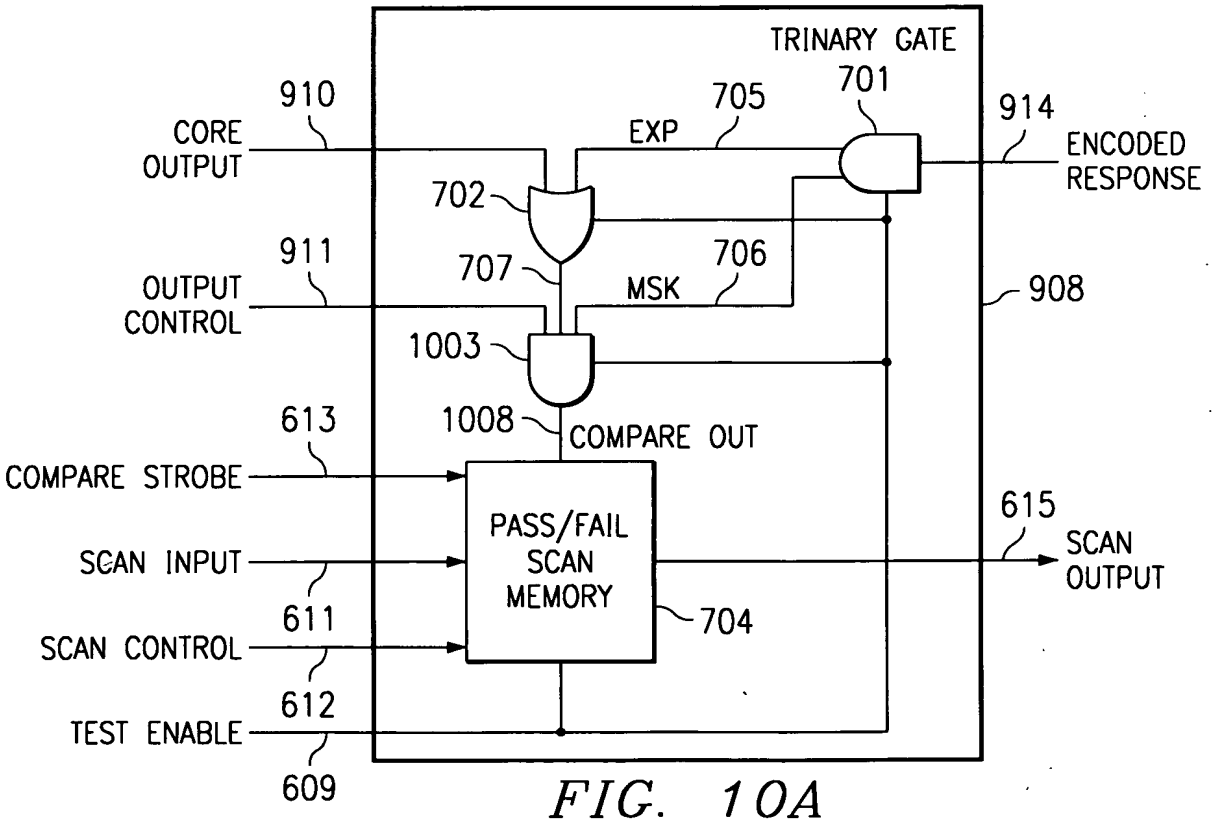


FIG. 10A

OC	TEN	ENR	MSK	EXP	FUNCTION PERFORMED
X	0	X	X	X	TEST DISABLED
1	1	GND	1	0	COMPARE LOW
1	1	VDD	1	1	COMPARE HIGH
1	1	1/2VDD	0	X	MASK COMPARE
0	1	GND/VDD	1	0/1	TEST OUTPUT CONTROL

FIG. 10B

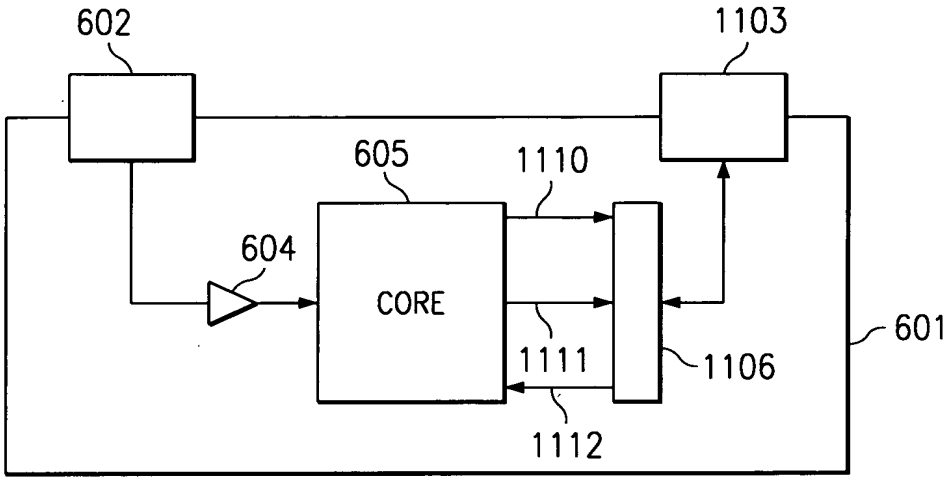


FIG. 11A

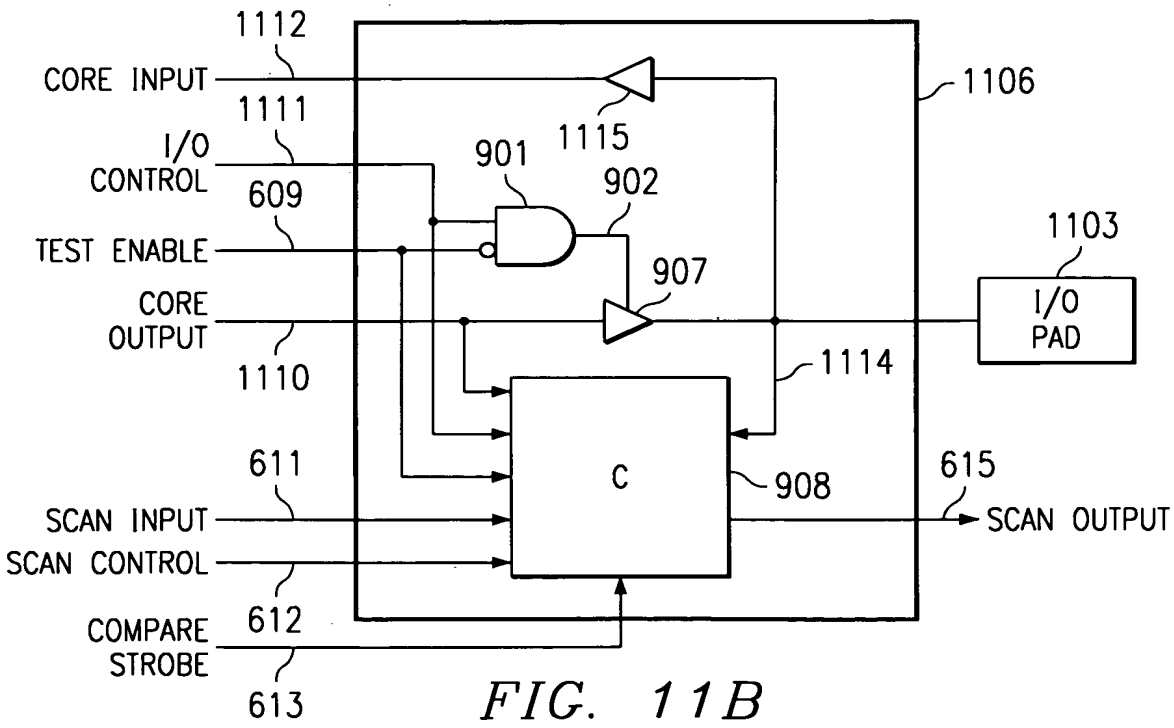


FIG. 11B

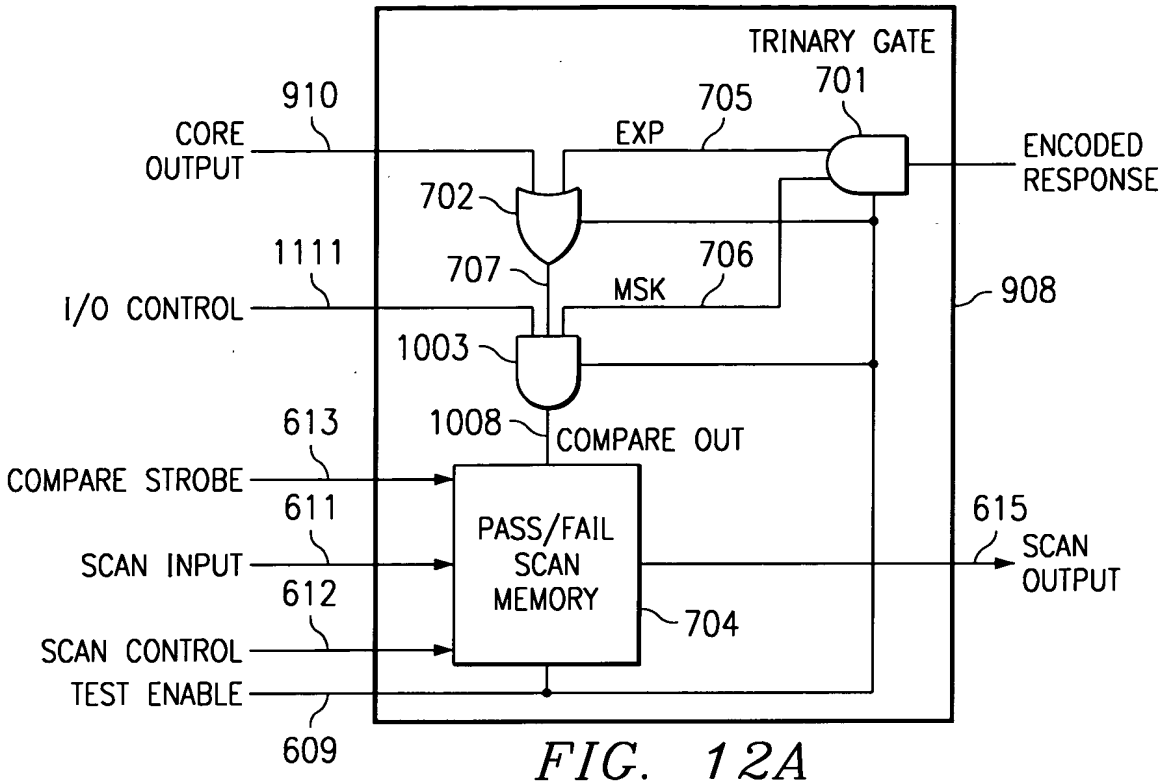


FIG. 12A

IOC	TEN	ENR	MSK	EXP	FUNCTION PERFORMED
X	0	X	X	X	TEST DISABLED
1	1	GND	1	0	COMPARE LOW
1	1	VDD	1	1	COMPARE HIGH
1	1	1/2VDD	0	X	MASK COMPARE
0	1	GND/VDD	1	0/1	TEST I/O CONTROL
0	1	GND/VDD	1	0/1	INPUT STIMULUS

FIG. 12B

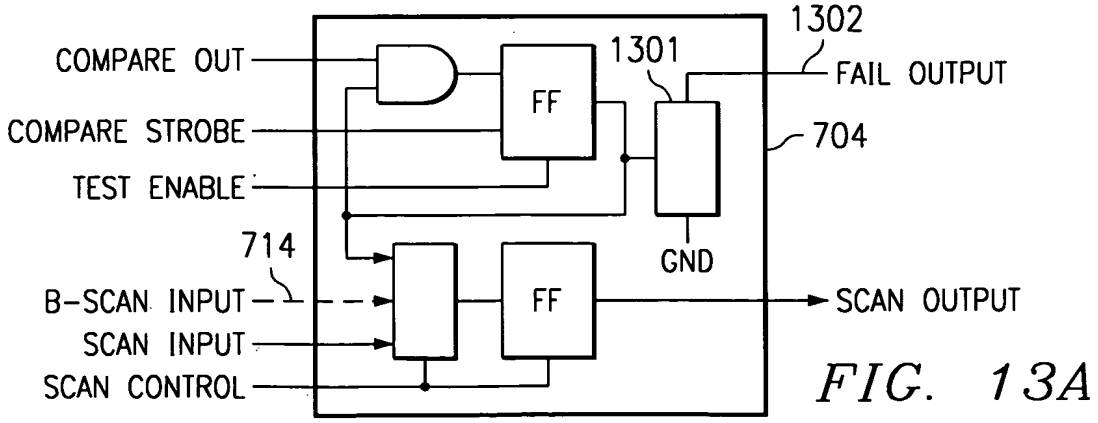


FIG. 13A

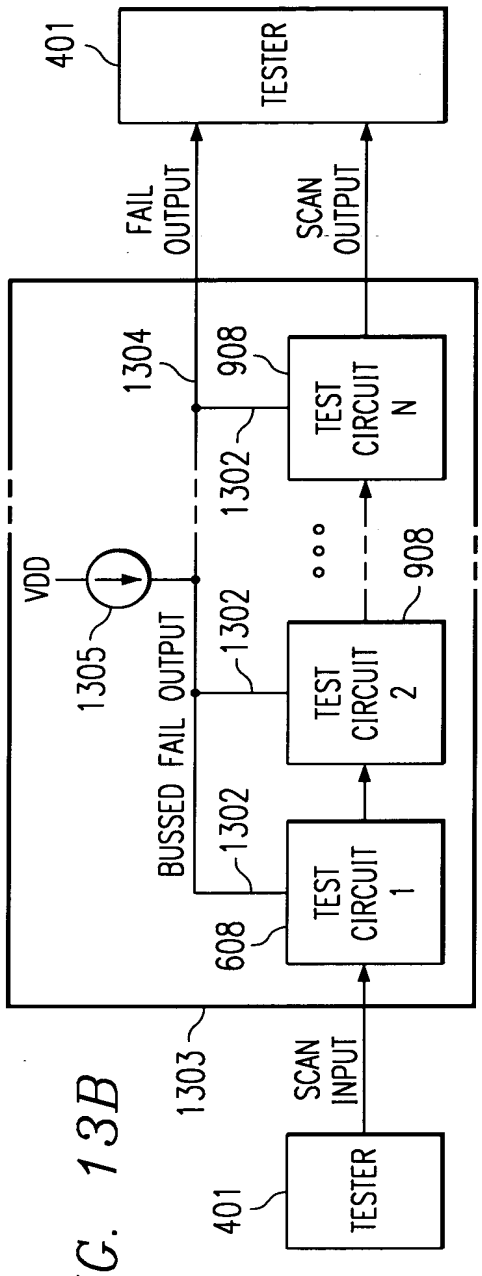


FIG. 13B

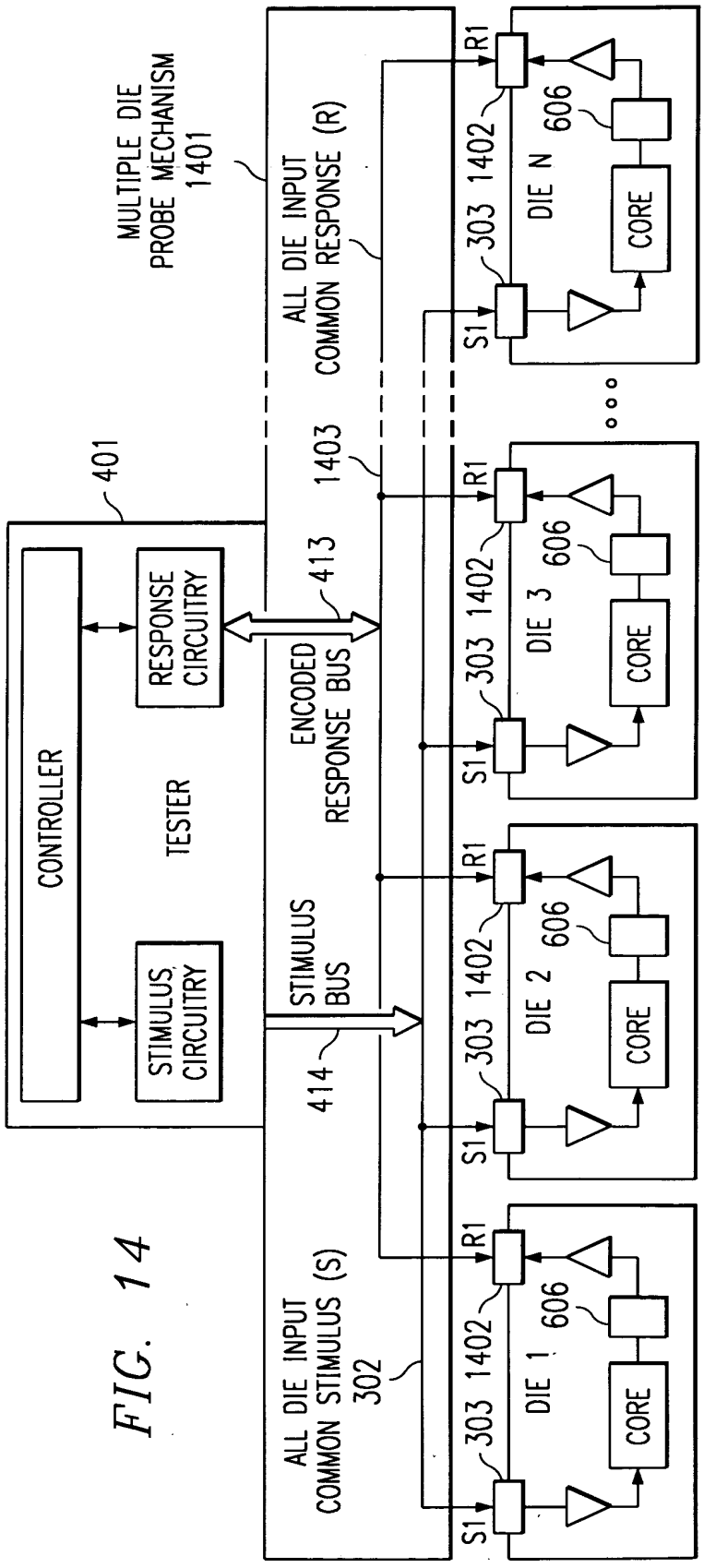
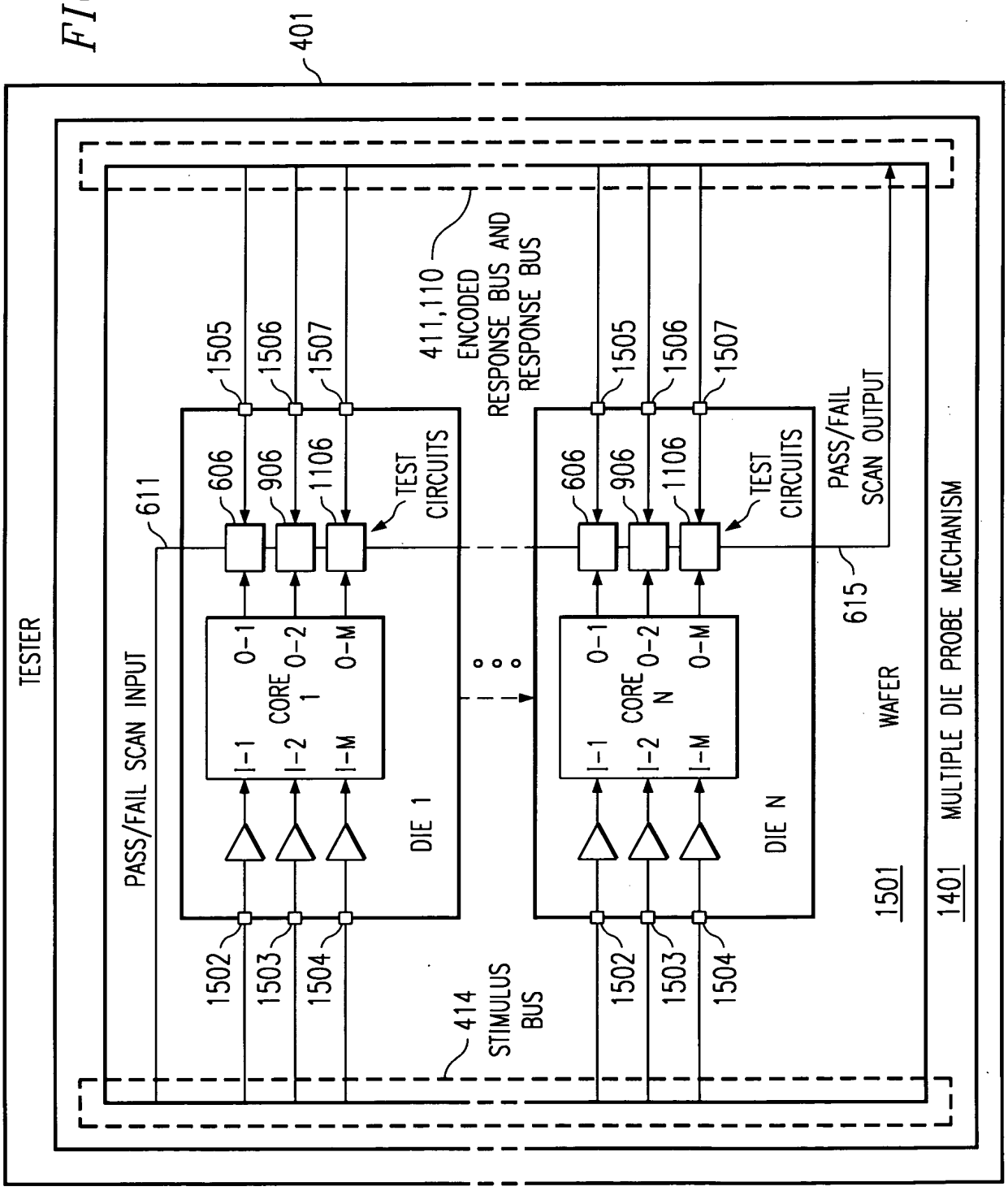


FIG. 14

FIG. 15


401
TESTER
PASS/FAIL SCAN INPUT
611
411,110
ENCODED
RESPONSE BUS AND
RESPONSE BUS
1505
1506
1507
606
906
1106
TEST
CIRCUITS
CORE
1
CORE
N
I-1
I-2
I-M
O-1
O-2
O-M
DIE 1
DIE N
1502
1503
1504
414
STIMULUS
BUS
615
PASS/FAIL
SCAN OUTPUT
WAFER
1501
1401
MULTIPLE DIE PROBE MECHANISM

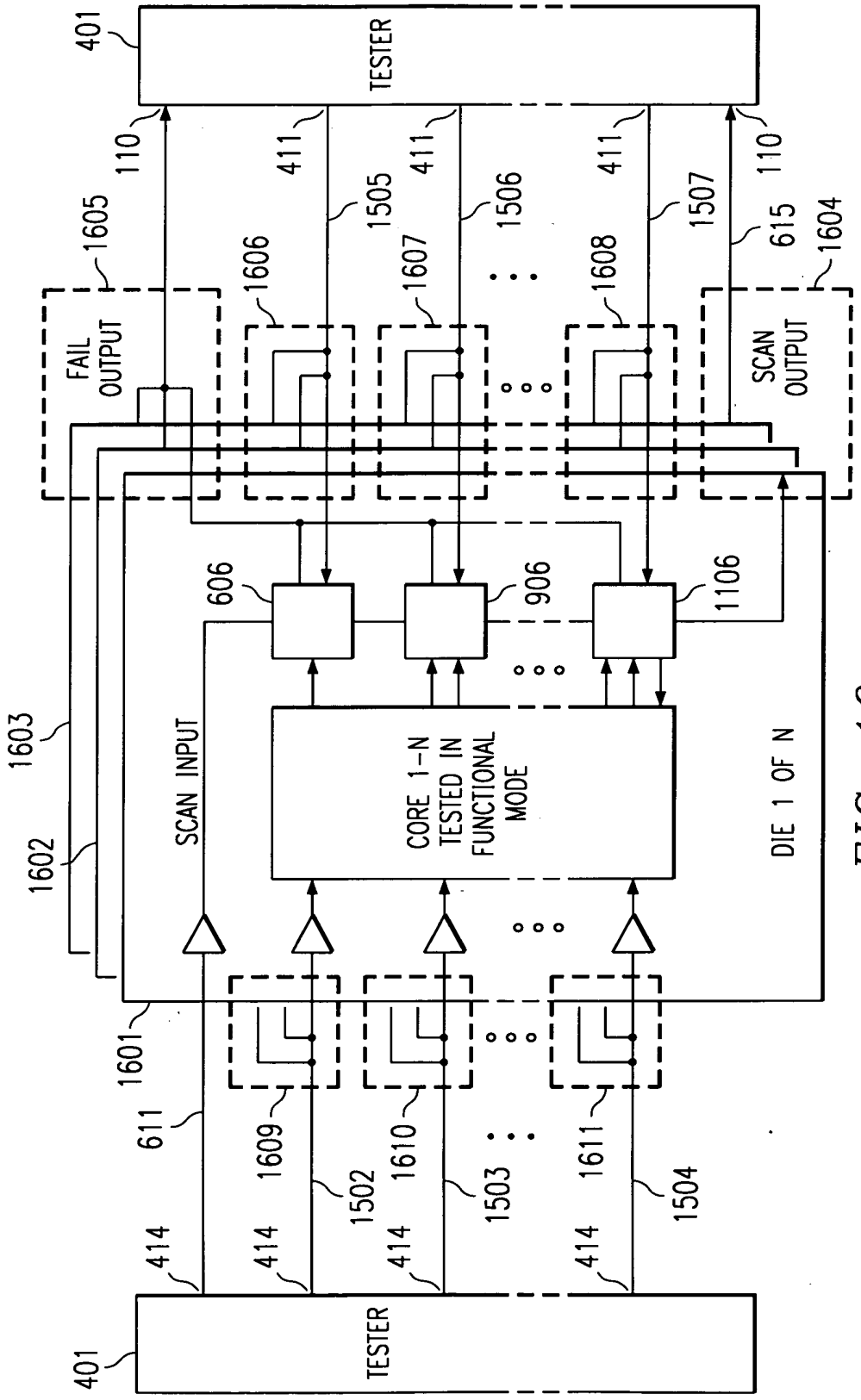


FIG. 16

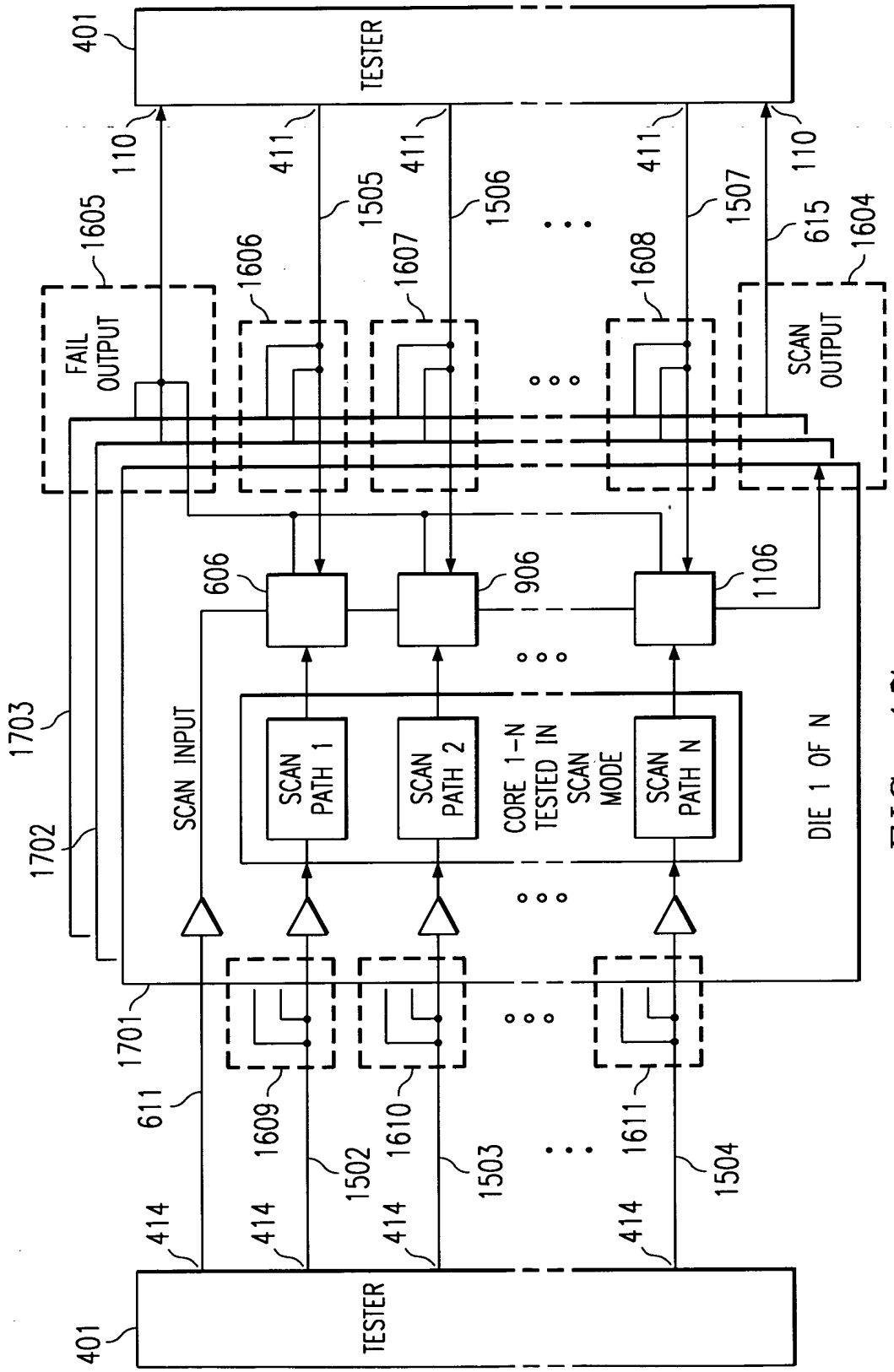


FIG. 17

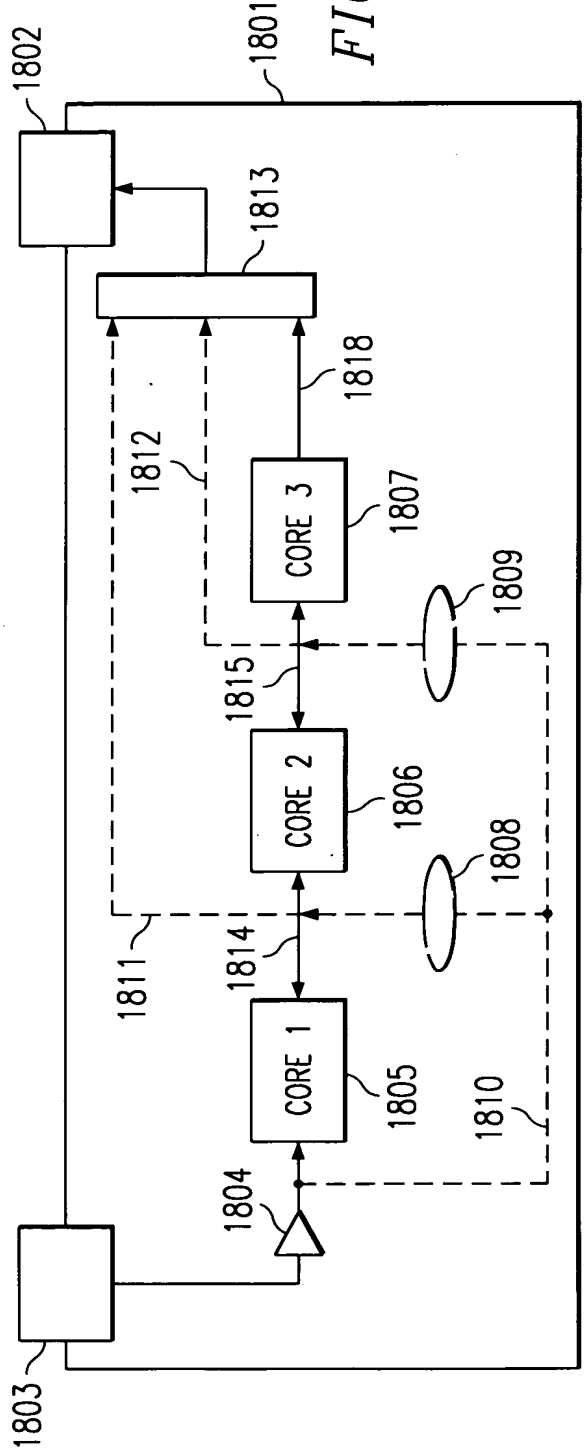


FIG. 18A

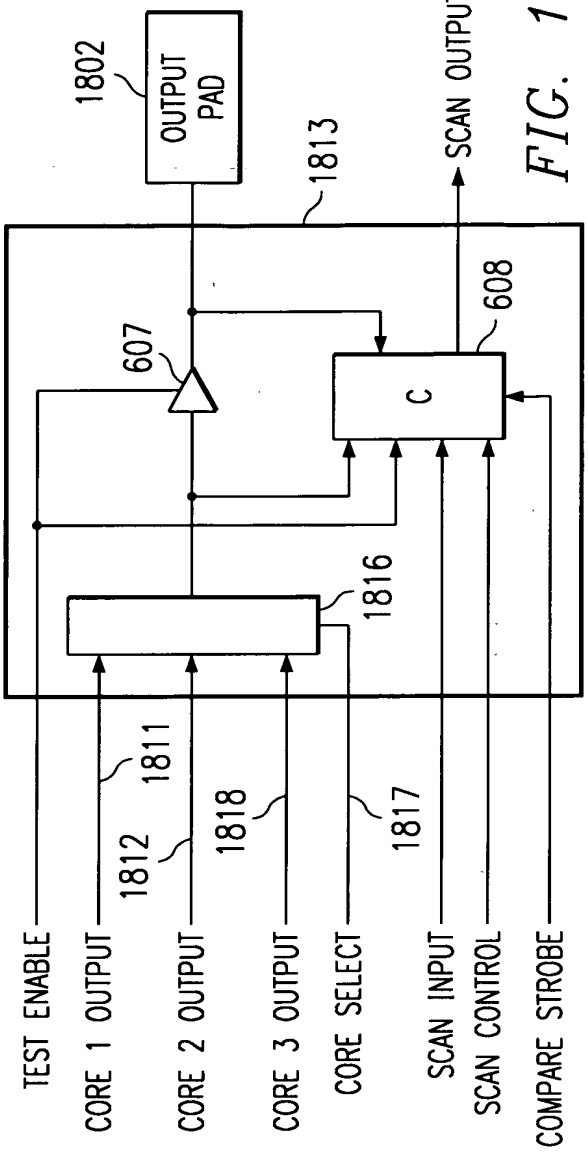


FIG. 18B

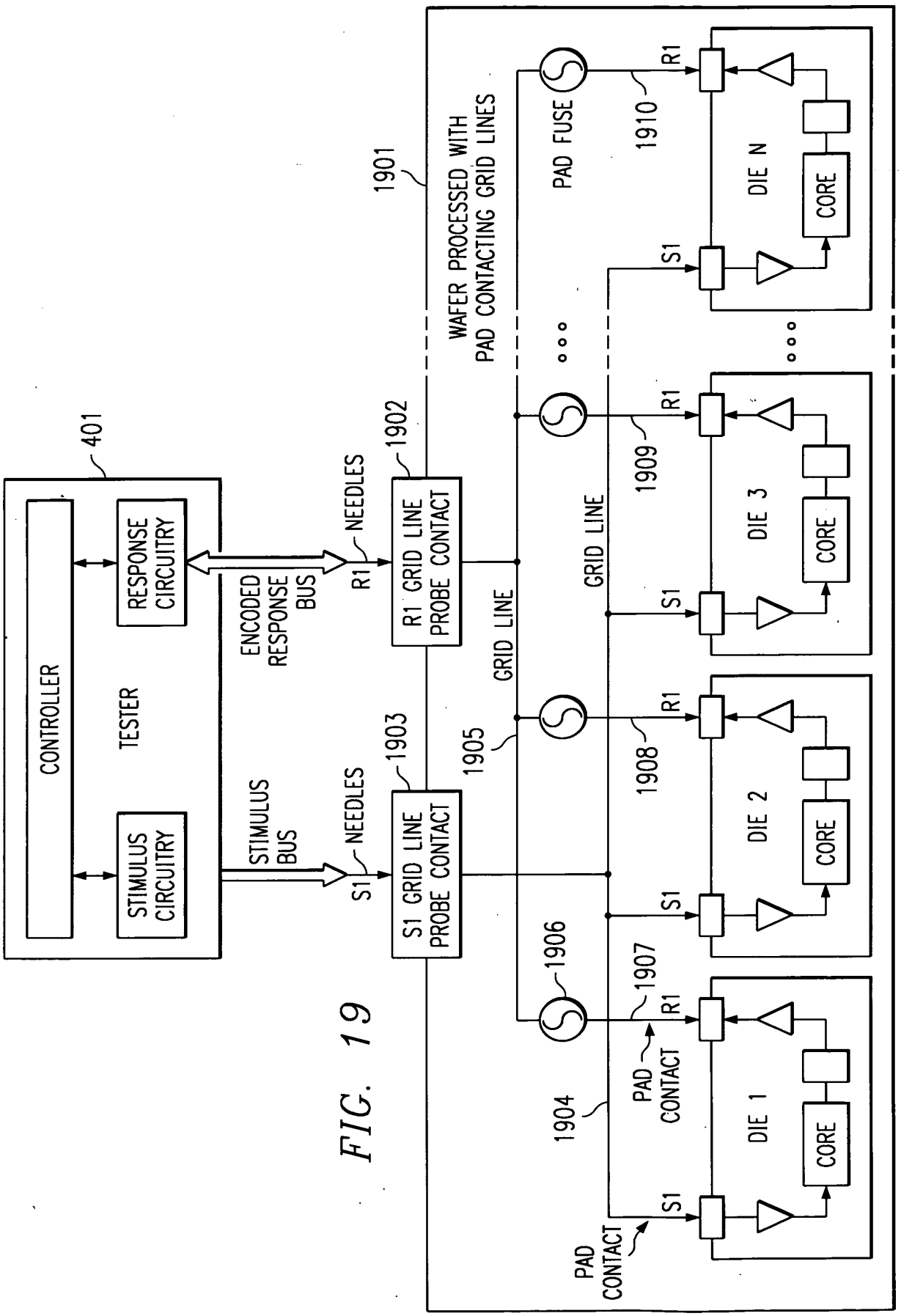


FIG. 19

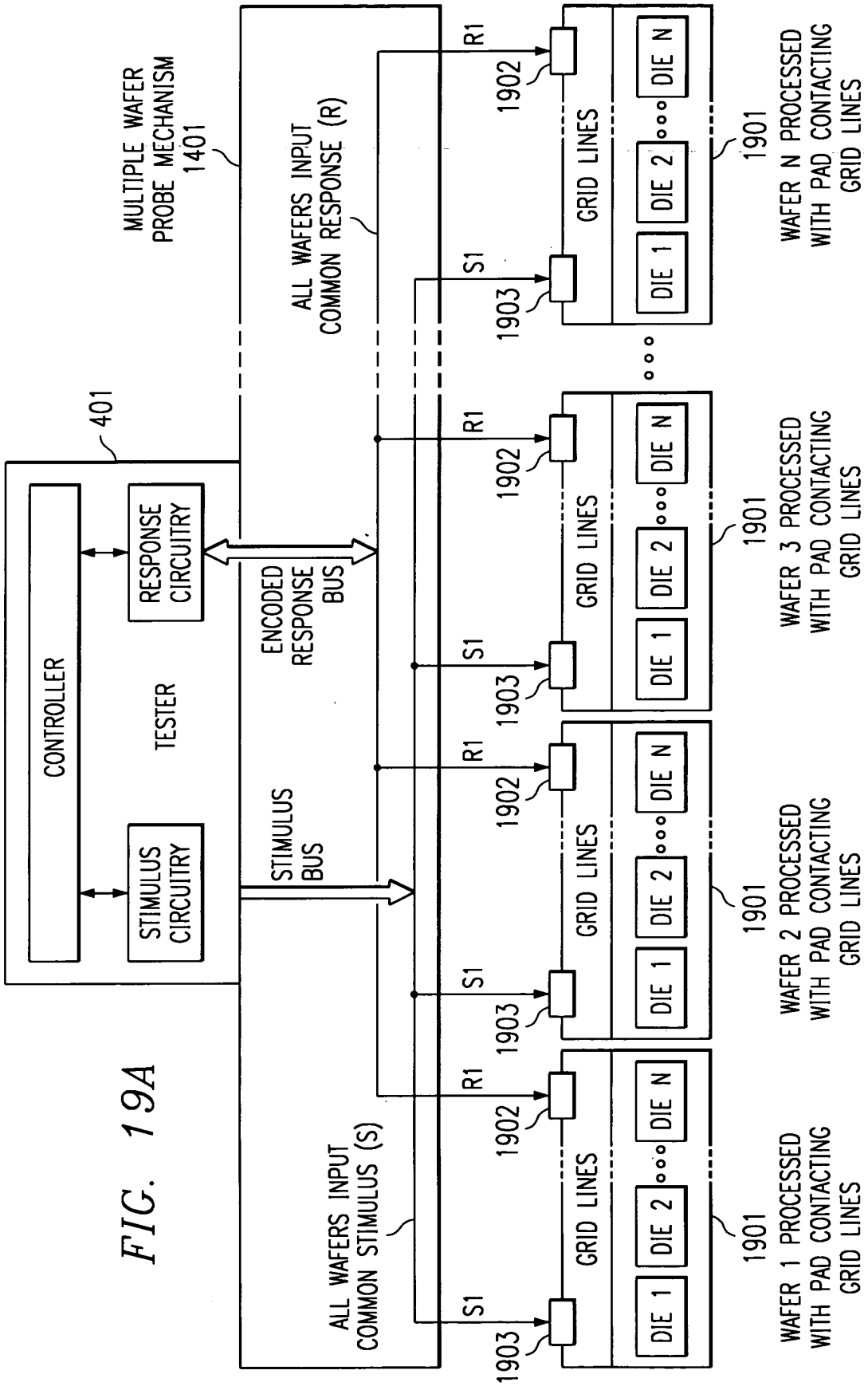


FIG. 19A

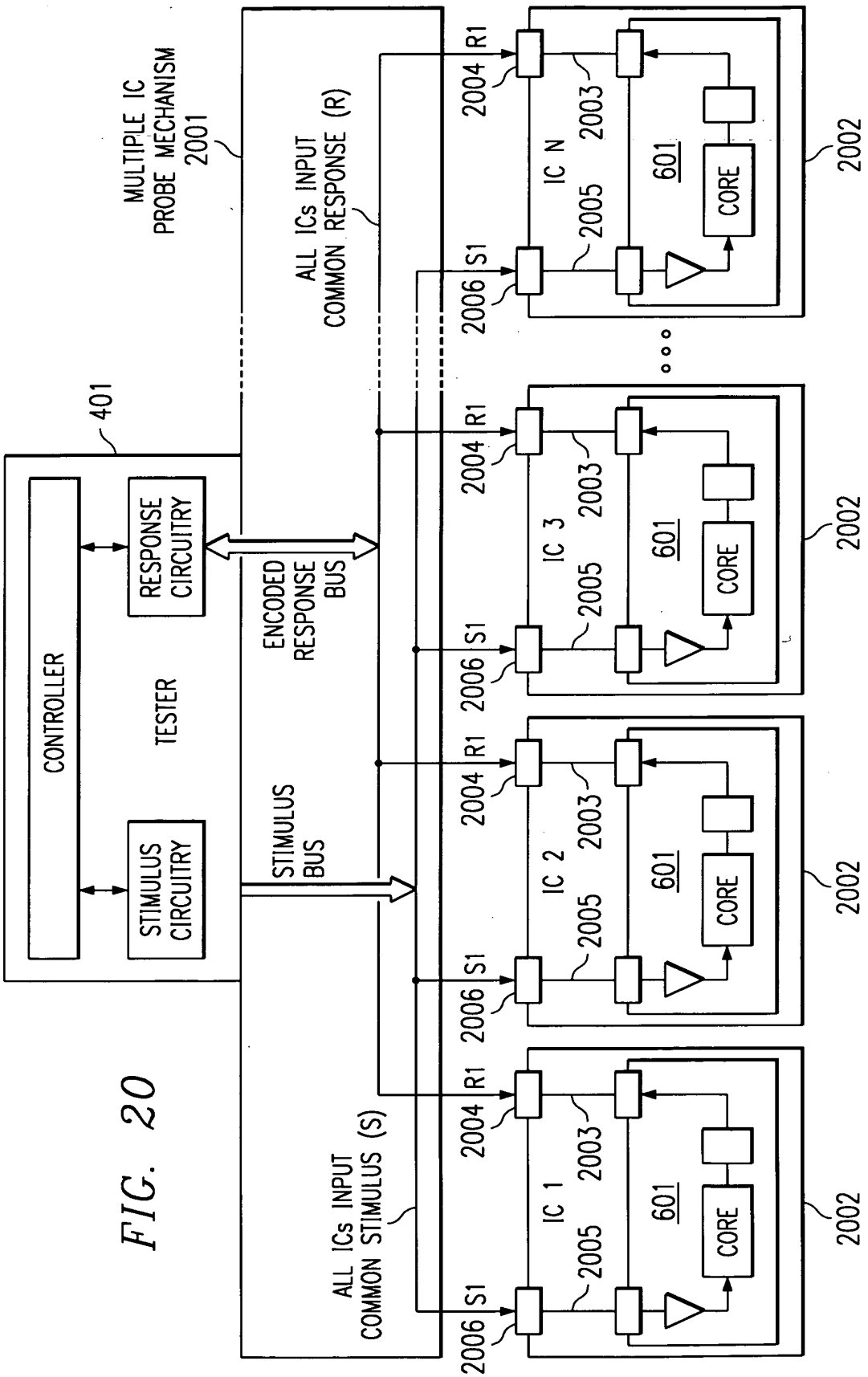


FIG. 20